FABRICATION METHOD OF SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

BACKGROUND OF THE INVENTION

The present invention relates to the technology for fabricating a semiconductor integrated circuit device and especially, relates to the technology useful in applying to fabrication of the semiconductor integrated circuit device, which including a step for polishing a thin film deposited on the surface of a semiconductor wafer by the chemical-mechanical polishing (CMP) method.

One of micro-fabrication technologies, which pay an important role in packaging integrated circuits on semiconductors at higher densities and in enhancing their performance, is the chemical-mechanical polishing method, for example, being used for formation of grooves isolating between elements referred to as Shallow Groove Isolation (SGI), planarization of interlayer dielectrics in a multilayer wiring formation step, and formation of embedded metal wiring. This chemical-mechanical polishing technology is described, for example, in the US Patent No. 4944836.

The chemical-mechanical polishing method is the method, by which the surface of a wafer is polished while polishing slurry is supplied on a turn table, on which a polishing pad made of hard resin is attached and particulate abrasive, such as silica (silica oxide), is used for the polishing slurry by

dispersing them in the deionized water and adding an alkaline substance for pH control.

However, such a problem has been pointed out that micro scratches may occur on the wafer surface by coagulated coarse particles when the wafer is polishing with the polishing slurry containing silica oxide, causing a deterioration in LSI manufacturing yield rate and reliability.

In Japanese Unexamined Patent Publication No. Hei 10(1998)-321588 (Kou et al.), one of methods was disclosed for preventing micro scratches from occurring on the wafer surface by coagulated particles. According to this Publication, generally, in the chemical-mechanical step, deionized water is supplied on the polishing pad to keep a wet condition continuously. In the polishing step, the polishing slurry is supplied on the polishing pad moistened with deionized water. However, the pH value of the polishing slurry containing silica oxide is about 10-11 while the pH value of purifies water is 7. For this reason, when the polishing slurry is supplied on the polishing pad moistened with deionized water, a large difference in the pH value between the polishing slurry and deionized water causes coarse coagulated particles to be created in the polishing slurry, leading to micro scratches on the wafer surface.

To solve this problem, in the above-mentioned Publication, such a method has been proposed that the polishing pad is

moistened with pH pre-adjusted deionized water so that its pH value is identical to that of the polishing slurry and then the polishing slurry is supplied on the polishing pad. In addition, another method has been proposed that a mixture of pH pre-adjusted deionized water and the polishing slurry mixed at a given ratio is prepared for supplying to the polishing pad. When an alkaline substance is used for the polishing slurry, an alkaline reagent should be used for the pH adjustment reagent while when an acid substance is used for the polishing slurry, an acid reagent should be used for the pH adjustment reagent. If the alkaline polishing slurry containing silica oxide is used, KOH or NH_4OH may be preferably used for the pH adjustment reagent.

SUMMARY OF THE INVENTION

Recently, to facilitate micro-fabrication of LSI elements and multilayer wiring, the chemical-mechanical polishing method has been applied in several steps of the wafer fabrication process. For example, in the step for forming an element isolating groove, dry-etching is applied to the primary surface of the wafer using a oxidation-resistant film as a mask to form the groove in the element isolating region, a silicone oxide film with a thickness larger than the depth of the groove is deposited on the primary surface of the wafer including the inside of the groove, chemical-mechanical polishing is applied

to the silicone oxide film using the oxidation-resistant insulating film as a stopper against polishing, and then the silicon oxide film is selectively left inside the groove to form the element isolating groove.

In the above-mentioned chemical-mechanical polishing step, generally, the polishing slurry having silica particles dispersed in water is used. Since on the surfaces of silica particles, hydrophilic Si-OH groups exist, inter-particle hydrogen bonding in the Si-OH group and the van der Waals force cause primary particles to coagulate each other when silica particles are dispersed in water, forming the coagulated particles (secondary particles) with a diameter larger than that of a single particle. Accordingly, in the polishing slurry having silica particles (dispersoid) dispersed in water (Dispersion medium), an abrasive component is composed of these coagulated particles.

If its diameter is rather small, the coagulated particles have no problem. However, in the actual polishing slurry, coarse coagulated particles with a diameter of 1 μm or larger (in this application, the coagulated particles with a diameter of 1 μm or larger are especially referred to as "coarse coagulated particles") exist and cause minute scratches called "micro scratches" to occur on the wafer surface, leading to a deterioration in yield rate or reliability. For example, in the above-mentioned step for forming element isolating grooves, if

the micro scratches occur on the surface of the oxidization-resistance insulating film while chemical-mechanical polishing is applied to the silicone oxide film using the oxidation-resistant insulation film as a stopper against polishing, some of the micro scratches may reach a underlying silicone substrate, causing damage on the substrate surface.

Although filtration of the polishing slurry is useful to some extent for removing the coarse coagulated particles in the polishing slurry, coagulated particles begin to re-coagulate in the polishing slurry if it is left as it is after the coarse particles are removed, which means that this method is not a fundamental means.

In this context, the inventor et al. has proposed the method to prevent the micro scratches from occurring on the wafer surface by the coagulated particles in advance (Patent Application No. 2000-145379). In this method, prior to the chemical-mechanical polishing step by supplying the polishing slurry on the wafer surface to be processed, the polishing slurry is left at rest for a given period to reduce the concentration of the coagulated silica particles with a diameter of 1μm or larger contained in the polishing slurry below 200,000/0.5cc, preferably 50,000/0.5cc, and more preferably 20,000/0.5cc.

The above-mentioned method proposed by the inventor can very efficiently reduce the concentration of coarse coagulated

silica particles contained in the polishing slurry. However, since the still-standing period is not always fixed due to a difference in manufacturing lot of the polishing slurry, it may not be expected that the method can reduce the concentration of coarse coagulated particles sufficiently if it is exclusively used.

An objective of the present invention is to provide the technology, which allows a reduction in density of coagulated particles contained in the polishing slurry to be used in the chemical-mechanical polishing step.

Another objective of the present invention is to provide the chemical-mechanical polishing technology, which allows a reduction in occurrence of micro scratches.

Another objective of the present invention is to provide the technology, which can control a reduction in yield rate and reliability of an integrated circuit device caused by micro scratches occurring in the chemical-mechanical polishing step.

The above-mentioned and other objectives and novel characteristics may be clarified by referring the descriptions of the specification and the attached drawings.

Out of the inventions to be disclosed in this application, typical ones are in brief explained below.

A fabrication method of a semiconductor integrated circuit device, which is one of the inventions of this application comprising steps of:

(a) preparing a polishing slurry in the stable particle dispersion state;

(b) diluting the polishing slurry with a water solution, which has deionized water as a main component; and

(c) supplying the polishing slurry on the surface of the wafer undergoing the mass-production process immediately after being diluted with the water solution to apply the chemical-mechanical polishing method.

Note that in this application, chemical-mechanical polishing (CMP) is the polishing method, in which generally, the wafers are moved in the bi-direction to polish while the polishing slurry is supplied with the wafer surface to be polished in contact with a polishing pad made of a sheet material such as soft cloth one another.

The polishing slurry is a fluid-colloidal suspension, in which generally, abrasive particles (dispersion medium) are mixed in water and a chemical etching agent (dispersoid). The abrasive particles generally indicate silica, ceria, zirconia, and alumina.

The insulating film isolating groove formed by polishing for smoothing is a element isolating groove, which is formed by selectively leaving the insulating film, of which surface is smoothed by chemical-mechanical polishing, inside the groove. Accordingly, the element-isolating grove, which is formed simply by depositing the insulating film inside the groove, is

not competent for the insulating film groove smoothed by polishing given here. For example, the element-isolating groove commonly referred to as Shallow Groove Isolation (SGI) or Shallow Trench Isolation (STI) is competent for it.

Deionized water includes not only "deionized water" used in the semiconductor fabricating process but also water solutions and chemical solutions containing deionized water as a main component.

In this application, the mass-production process on the wafer line means the process, in which a throughput/day for the specific chemical-mechanical polishing system used on the wafer line is at least 25 or more or 50 or more 8/inch wafers and more generally 100 wafers or more. Note that it goes without saying that this critical number of wafers is inversely proportional to the wafer areas.

In addition, in the following embodiments, if necessary for convenience, members are explained across more than one section or embodiment, however, they are not independent of each other, with a exception specified otherwise, one partially or completely explains the example another mode, details, and supplements of the other.

In addition, in the following embodiments, when the number of members (including number of units, values, quantities, ranges, etc.) is referred to, it is not needed to limit to the given number and it may be above or lower the

specified number with an exception of such a case that the number is specifically defined or it is clear that the number is limited to the specific number principally. In addition, in the following embodiments, it goes without saying that the components (including the number of component steps) are not always requisite with an exception of such a case that they are especially specified or it is clear that they are requisite principally.

Similarly, in the following embodiments, when the shapes and relative positions of the members are referred to, they may include those substantially close to or similar to the shapes and relative positions with an exception of such a case that they are especially specified or it is perhaps clear that they are not correct principally. This is applicable to above-mentioned values and ranges.

In this application, when the semiconductor integrated circuit device is referred to, it may include not only those specially fabricated on a monocrystal silicone substrate but also those fabricated on other substrates such as a Silicone On Insulator (SOI) substrate and Thin Film Transistor (TFT) substrate for manufacturing liquid crystal. Moreover, the wafer is a monocrystal silicone substrate (usually, almost disk-shape), SOI substrate, glass substrate, other insulation substrate, semi-insulation substrate, semiconductor substrate or complex of any of them.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig.1 is a main sectional view of a silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.2 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.3 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.4 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.5 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.6 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present

invention.

Fig.7 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.8 is a schematic drawing showing a processing part of a chemical mechanical polishing system, which is used to polish chemo-mechanically silicone oxide films.

Fig.9 is a schematic drawing showing a slurry supply pipe of the chemical mechanical polishing system shown in Fig.8.

Fig.10 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.11 is a graph showing the result of evaluating the relationship between a scratch defect density and a polishing slurry concentration.

Fig.12 (a) and Fig.12 (b) are graphs showing the results of evaluating the relationship between the scratch defect density and the polishing slurry concentration.

Fig.13 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.14 is a main sectional view of the silicone substrate

showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.15 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.16 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.17 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.18 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.19 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.20 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated

circuit device according to one embodiment of the present invention.

Fig.21 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

Fig.22 is a main sectional view of the silicone substrate showing the method for fabricating a semiconductor integrated circuit device according to one embodiment of the present invention.

PREFERRED EMBODIMENTS OF THE INVENTION

The embodiments of present invention are explained below in detail based on drawings. note that in all the drawings used to explain the embodiments, the same signs are assigned to the same members and repeated explanation for them is omitted.

Embodiment 1

A fabrication method of Dynamic Random Access Memory (DRAM), which is the embodiment 1 of the present invention, is explained in an order of steps based on Fig.1 - Fig.22.

First, as shown in Fig.1, after a wafer 1 made of p-type monocrystal silicone with a resistivity, for example, 1 - 10 Ωcm is heat-oxidized at a temperature of about 850℃ and on its surface, a thin silicone oxide film 2 with a thickness of about 10nm is formed, on the top of the silicone oxide film 2,

a silicone nitride film (oxidation-resistant film) 3 with a thickness of about 120nm is deposited by the CVD method.

The silicone nitride film 3 is used as a mask when a groove is formed by etching the substrate 1 in an element-isolating region. In addition, the silicone nitride film 3 is used as a mask, which prevents the surface of the underlying substrate 1 from being oxidized because it has a characteristic difficult to be oxidized. The silicone oxide film 2 under the silicone nitride film 3 is formed so that a stress exerted on an interface between the substrate 1 and the silicone nitride film 3 is relieved to prevent any fault such as displacement from occurring due to the stress on the surface of the substrate 1.

Next, as shown in Fig.2, after the silicone nitride film 3 and the underlying silicone oxide film 2 are selectively removed from the element-isolating region by dry-etching using a photo-resist 4 as a mask, as shown in Fig.3, the groove 5a with a depth of about 350nm is formed on the substrate 1 in the element isolating region by dry-etching using the silicon nitride film 3 as a mask.

Next, after the photo-resist 4 is removed, as shown in Fig.4, the substrate 1 is heat oxidized at a temperature of about 800 - 1000℃ to form a thin silicone oxide film 6 with a thickness of about 10nm on the inner wall of the groove 5a. The silicone oxide film 6 is formed so that any damage inside the inner wall of the groove 5a caused by dry-etching can be recovered and a

stress exerted on the interface between a silicone oxide film 7, which is embedded inside the groove 5a in a later step, and the substrate 1 can relieved.

Next, as shown in Fig.5, the silicone oxide film 7 is deposited on the substrate 1 including the inside of the grove 5a by the CVD method. The silicone oxide film 7 is deposited at a thickness larger than the depth of the groove 5a (for example, about 500 - 600 nm) to embed the silicone oxide film 7 inside of the groove 5a with no gap. The silicone oxide film 7 should be composed of a film with a high level of step coverage, for example, a silicone oxide film (hereafter, simply referred to as P-TEOS) formed by the plasma CDV method using oxygen and $(C_2H_5)_4Si$.

Next, after the substrate 1 is heat oxidized at a temperature of about 1000℃ to densify for improving the quality of the silicone oxide film 7 embedded inside the groove 5a, as shown in Fig.6, the silicone oxide film 7 on the silicone nitride film 3 is dry-etched using the photo-resist 8 formed on the groove 5a as a mask. This application of dry etching is intended to make the height of the surface of the silicone oxide film 7 almost identical both on the groove 5a and on the silicone nitride film 3.

Next, as shown in Fig.7, after the photo-resist film 8 on the silicone oxide film 7 is removed, chemical-mechanical polishing is applied to the silicone oxide film 7 by the

following method.

Fig.8 is a schematic drawing showing a processing part of the chemical-mechanical polishing system 100 used for polishing the silicone oxide film 7. As known from the figure, a turntable 101 is disposed at the processing part of the chemical-mechanical polishing system 100 for polishing the wafer (substrate) 1 by the single wafer polishing method.

The turntable 101 is rotationally driven in the horizontal plane by a driving mechanism (not shown). In addition, on the top of the turntable 101, a polishing pad 102 made of porous synthetic resin such as polyurethane is attached.

Above the turntable 101, a wafer carrier 103, which is rotationally driven up and down and in the horizontal plan by the driving mechanism (not shown) is disposed. The wafer 1 is supported with its primary surface (surface to be polished) faced down by a retainer ring 104 and a membrane 106 disposed under the wafer carrier 103 and pressed against the polishing pad 102 under a given weight. Between the surface of the polishing pas 102 and the surface to be polished of the wafer 1, a polishing slurry S is supplied through a slurry transportation tube 105 to polish the surface to be polished of the wafer 1 chemically and mechanically.

Moreover, above the turntable 101, a dresser 107, which is rotationally driven up and down and in the horizontal plane by the driving mechanism (not shown), is disposed. At the bottom

of the dresser 107, a backing material, on which diamond particles are electrodeposited, is disposed and cuts the surface of the polishing pad 102 regularly to prevent clogging due to abrasive particles.

The polishing slurry S used in the embodiment is prepared by dispersing fumed silica which is an abrasive particle component, in water and adding NH_4OH to adjust its pH value. The polishing slurry S, after its components are adjusted in the following method, is supplied to a gap between the surface of the polishing pad 102 and the surface to be polished of the wafer 1.

First, the polishing slurry S, of which silica concentration has been adjusted so that silica dispersed in water might keep most stable, is prepared. Especially, the polishing slurry is prepared so adjusted that it contains 11 - 15 weight %, preferably 11 - 13 weight %, and more preferably 12 weight % of silica and its pH is kept about a value 11 (10.5 - 11.5) by adding NH_4OH.

Among the commercially available polishing slurry products, some products have silica concentration adjusted within a tolerance above-mentioned and they may be used. Note that the commercially available slurry products contain coarse coagulated particles with a diameter of 1μm or larger and foreign matters causing micro scratches, which is the problem to be solved by the present invention. Accordingly, it is

desirable that when the polishing slurry S purchased from a slurry supplier is supplied to the chemical-mechanical polishing system 100, a filter is installed in a pipe connecting the a tank containing the purchased slurry S and the chemical-mechanical polishing system 100 to sufficiently filter out the coarse coagulated particles and the foreign matters from the polishing slurry S.

In addition, to effectively restrain occurrence of micro scratches, the polishing slurry S supplied to the chemical-mechanical polishing system 100 should be left at rest for 30 days or more, preferable 40 days or more, and more preferable 45 days or more and used only after it is verified that the number of coarse coagulated particles with a diameter of 1 μm or larger contained 0.5cc of polishing slurry is below 200,000, preferable below 50,000, and more preferably below 20,000. Moreover, when the polishing slurry S, which was left at rest for the above-mentioned period, is transported from the tank into the chemical-mechanical polishing system 100, supernatant liquid should be skimmed from 5cm or more above and preferably 10cm or more above the bottom of the tank not to mix coarse coagulated articles and foreign matters deposited at the bottom of the tank.

Leaving the polishing slurry at rest means that the polishing slurry S filled up in the tank is left at rest with no operation such as vibration, stirring, and heating

(involving material transportation on a convection). Note that the method for storing the polishing slurry S described here is explained in detail in the Patent Application No. 2000-145379.

Next, in this embodiment, the polishing slurry S is diluted with deionized water. A mixture rate of 1 (polishing slurry) : 1 - 1.2 (deionized water) is used so that the concentration of silica contained in the polishing slurry S after dilution is 3 - 9 weight %, preferably 4 - 8 weight %, and more preferably 8 weight %. Note that some of commercially available polishing slurry products contain high concentrate of silica (for example, 25 weight%). If this type of polishing slurry S containing a high concentration of silica is used, the concentration of silica contained in the diluted polishing slurry is adjusted within the above-mentioned range by using a larger mixture rate of deionized water. Note that deionized water includes water solutions and chemical solutions mainly made of water, all of them are given a generic name "deionized water".

Thus, the concentration of coarse coagulated particles contained in the polishing slurry S is reduced by diluting the polishing slurry S with deionized water to increase its volume. Note that if the dilution rate of the polishing slurry S is increase, the concentration of coarse coagulated particles further decreases but it is preferable that the concentration

of silica contained in the diluted polishing slurry S is at least 3 weight % or more because the polishing rate is reduced when the concentration of abrasive component of the polishing slurry S decreases.

In addition, when the polishing slurry S is diluted with deionized water, the concentration of coagulated particles temporarily decreases and after the polishing slurry S being left at rest, silica particles begin to coagulate. Accordingly, the polishing slurry diluted with deionized water should be used for polishing as soon as possible. This means that dilution of he polishing slurry S is performed immediately before it is supplied in the gap between the polishing pad 102 and the surface to be polished of the wafer 1.

The time allowed for a period from dilution of the polishing slurry S with deionized water until application to polishing is up to about two hours and if this time period is exceeded, dilution ceases to be in effect because the concentration of coagulated particles returns to the level before dilution. Since re-coagulation of silica proceeds with time in the polishing slurry S, it is preferable that the time from dilution of the polishing slurry S until application to polishing is shorter and usually, it should be set to 10 minutes or less and preferably 10 - 15 seconds or less.

For example, as shown in Fig.9, the polishing slurry S diluted with deionized water can be rapidly supplied for

polishing by disposing a piping 105a for supplying the polishing slurry and a piping 105b for supplying deionized water inside a slurry supply pipe to mix the polishing slurry S and deionized water at an end of the slurry supply pipe 105.

Alternately, a deionized water supply pipe may be disposed independently of the slurry supply pipe 105 on the polishing pad 102 to mix deionized water supplied from the deionized water supply pipe and the polishing slurry S supplied from the slurry supply pipe 105 on the surface of the polishing pad 102. Moreover, it may be possible that after the polishing slurry S is supplied on the surface of the polishing pad 102, deionized water is supplied on the polishing pad 102 for mixing them. Note that since the ratio between them loses partially balance if the polishing slurry S and deionized water are mixed on the surface of the polishing pad 102, an imbalance may occur in the amount of polishing in the wafer plane.

After the substrates (wafers) 1 undergoing the mass-production process are transported to the processing part of the chemical-mechanical polishing system 100 one by one and supported at the bottom of the wafer carrier 103, the silicone oxide film 7 deposited on the substrate is polished with the diluted polishing slurry S. The polishing conditions are set to, for example, load=250g/cm_2, wafer carrier revolutions=30rpm, turn table revolutions=25rpm, and slurry flow rate=200cc/min.

Fig.10 shows a cross section of the substrate (wafer) 1 immediately after chemical-mechanical polishing has been applied to it. Polishing of the silicone oxide film 7 is performed using the silicone nitride film 3 as a stopper and stopped when the thickness of the silicone nitride film 3 reaches 60nm. This forms an element-isolating groove 5, in which the silicone oxide film 7 is embedded, in the element-isolating region of the primary surface of the substrate (wafer) 1.

The polished substrates (wafers) 1, after being taken out from the wafer carrier 103, are transported to cleaning equipment (not shown) connected to a subsequent stage of the chemical-mechanical polishing system 100 one by one and silica abrasive particles and alkaline metal ions contained in the polishing slurry S are removed by deionized water cleaning, deionized water ultrasonic cleaning, deionized water flush cleaning, or deionized water spin cleaning. In addition, they are dried by any method such as spin-dry or IPA (Isopropyl alcohol) vapor dry and then are transported to the next step. On the other hand, new substrates (wafers) 1, which have undergone the step shown in Fig.7, are transported to the chemical-mechanical polishing system 100 one by one and the chemical-mechanical polishing step is repeated.

Fig.11 is a graph showing the comparison of the defect density values of scratches on the surfaces of the wafers 1 occurring in the step for forming the element isolating groove

between the case where the polishing slurry (silica concentration=6 weight%) diluted with deionized water is used and the case where the undiluted polishing slurry (silica concentration=12 weight%) is used. The vertical axis indicates the scratch defect density values measured using automatic wafer visual inspection equipment (WI-800) from Hitachi Tokyo Electronics and the horizontal axis is inspection dates. As shown in the figure, the scratch defect density values are undoubtedly smaller on the day when the polishing slurry diluted with deionized water was used or later then those before the day.

Fig.12 is a graph showing the comparison of the numbers of macro scratches between the case where the polishing slurry (silica concentration=6 weight%) diluted with deionized water is used on the primary surface of the mirror wafer, on which the silicone oxide film was deposited by the plasma CVD method, (Fig.12(a)) and the case where the undiluted polishing slurry (silica concentration=12 weight%) is used (Fig.12(b)). The number of micro scratches was measured using visual inspection equipment (LS-6510) from Hitachi DECO. As shown in the figure, the number of micro scratches is clearly smaller in the wafers polished using the polishing slurry diluted with deionized water than that of wafers using the undiluted polishing slurry.

Next, the step after the formation of the element-isolating groove 5 is described below in brief. First, as shown

in Fig.13, after the silicone nitride film 3 is removed from the substrate 1 using hot phosphorous acid and the silicone oxide film 2 under the silicone nitride film 3 is removed using hydrofluoric acid, the substrate 1 is heat-oxidized at a temperature of about 800 - 1000℃ to form a thin film of silicone oxide 10 with a thickness of 10nm on the surface of the active region.

As shown in Fig.14, boron (B) is ion-implanted on the substrate 1 through the silicone oxide film 10 to form a p-type well 9, the silicone oxide film 10 is removed using hydrofluoric acid, and then the substrate 1 is heat-oxidized at a temperature of about 800 - 850℃ to form a clean gate oxide film 11 with a thickness of about 6 - 8nm on the surface of the active region.

Next, as shown in Fig.15, a gate electrode 12 (word line WL) is formed on the gate oxide film 11. The gate electrode 12 (word line WL) is formed by, for example, depositing a polycrystalline silicone film with a thickness of about 50nm, in which phosphorus (P) is doped, on the gate oxide film 11 by the CVD method, depositing a WSi_2 (tungsten silicide) with a thickness of about 120nm by the spattering method on the silicone film surface, depositing a silicone nitride film 13 with a thickness of about 160nm on the WSi_2 surface by the CVD method, and then by patterning these films by dry etching using a photo-resist film (not shown) as a mask.

Next, after the surface of the gate oxide film 11 is cleaned with hydrofluoric acid to remove etching waste, as shown in Fig. 16, phosphorus (P) or arsenic (As) is ion implanted in the p-type well 9 to form a n-type semiconductor region 14 (source, drain). In the steps up to this point, a MISFETQs for DRAM memory selection has been almost fabricated.

Next, as shown Fig.17, after the silicone nitride film 15 is deposited on the substrate 1 by the CVD method and a spin-on glass film 16 is spin-coated on the silicone nitride film 15, the silicone oxide film 17 is deposited on the spin-on glass film 16 by the CVD method.

Next, as shown in Fig.18, the silicone oxide film 17 is chemically-mechanically polished and its surface is smoothed. In this polishing step, since scratches are increased on the spin-on glass film 16 by hydrofluoric cleaning in the next step if micro scratches occur on the silicone oxide film 17 and some of them reach the sub-layer spin-on glass film 16, plugs 20 may be shorted though scratches when plugs 20 are inserted into contact holes 18 and 19 formed on the spin-on glass film 16 in the later step. Accordingly, in this chemical-mechanical polishing step, the polishing slurry diluted with deionized water is used for polishing as described earlier.

Next, as shown in Fig.19, the silicone oxide film 17, the spin-on glass film 16, and the silicon nitride film 15 are dry etched using the photo-resist film (not shown) as a mask to form

the contact holes 18 and 19 over the n-type semiconductor region 14 (source, drain).

Next, after the insides of the contact holes 18 and 19 are cleaned with hydrofluoric acid, the plugs 20 is formed inside the contact holes 18 and 19. To form the plugs 20, for example, a low-resistance polycrystalline silicone film, in which P was doped, is deposited inside of the contact holes 18, 19 and over the silicone oxide film 17 by the CVD method, unnecessary portions of the polycrystalline silicone film over the silicone oxide film 17 are removed by dry etching (or chemical-mechanical polishing).

Next, as shown in Fig.20, after a silicone oxide film 21 is deposited over the silicone oxide film 17 by the CVD method and the silicone oxide film 21 over the contact hole 18 are etched to form a through hole 22, a plug 23 is formed inside the through hole 22. To remove the plug 23, for example, a TiN (titanium nitride) film and a W (tungsten) film are deposited over the silicone oxide film 21 and the unnecessary portions of the TiN film and W film over the silicone oxide film 21 are removed by chemical-mechanical polishing. Consequently, the W film, which is deposited over the silicone oxide film 21 by the spattering method, is pattered to form a bit line BL over the plug 23.

Next, after over the bit line BL, a silicone oxide film 24 is deposited by the CVD method and the silicone oxide film 24 is etched over the contact hole 19 to form a through hole

25, a plug 26 is formed inside the through hole 25. To form the plug 26, for example, a low-resistance polycrystalline silicone film, in which P was doped, is deposited inside the through hole 25 and over the silicone oxide film 24 by the CVD method and unnecessary portions of the silicone oxide film 24 are removed by dry etching (or chemical-mechanical polishing).

Next, as shown in Fig.21, after a silicone nitride film 27 is deposited over the silicone oxide film 24 by the CVD method and a silicone oxide film 28 is deposited over the silicone nitride film 27 by the CVD methods, the silicone film 28 and the silicone nitride film 27 under the film 28 are dry etched using a photo-resist film (not shown) as a mask to form a groove 29 over the through hole 25. A lower electrode 30 of a capacitance element C for information storage described later is formed along the inner wall of the groove 29 and to increase the quantity of built-up charges by enlarging the surface area of the lower electrode 30, it is required that the thick silicone oxide 28 be deposited.

Next, as shown in Fig.22, the capacitance element C for information storage having the lower electrode 30, a capacitance insulating film 31, and an upper electrode 32 is formed inside the groove 29. The lower electrode 30 is made of, for example, the P-doped low-resistance polycrystalline silicone film and the capacitance insulating film 31 is made of, for example, a tantalum oxide (Ta_2O_5) film. In addition,

the upper electrode 32 is made of a Tin film. In the steps up to this point, a memory cell, which is composed of the MISFETQs for memory cell selection and the capacitance element C for information storage connected to the MISFETQs in series, has been fabricated.

Thus, the present invention by the inventor has been especially described based on the embodiments and it goes without saying that the present invention is not limited to the above-mentioned embodiments and various modifications may be made to it within a range without derogating from its intent.

The effects achieved by typical ones out of the inventions disclosed in this application are explained below in brief.

Since micro scratches can be reduced by diluting the polishing slurry with deionized water to lower the concentration of coagulated particles immediately before the surface of the wafer is polished using the chemical-mechanical polishing method, the yield and reliability of a semiconductor integrated circuit device can be improved.